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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,719	12/15/2000	Kenneth L. Graber	LMCO.03PA	1468

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EXAMINER	
SHANNON, MICHAEL R	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,719	GRABER ET AL.	
	Examiner	Art Unit	
	Michael R. Shannon	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 31-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,13-26,31 and 32* is/are rejected.

7)☒ Claim(s) *4-12 and 33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10 January 2005 regarding the rejections of claims 1-3, 13, 17, 18, and 19 have been fully considered but they are not persuasive.

Regarding the arguments set forth at the bottom of page 9 of the applicant's remarks, the applicant states "Dunn's system does not appear to allow selection of one to at least two video streams for output by a single terminal controller". As stated by the applicant and agreed to by the Examiner, Dunn's adapter modules 1000 do appear to select only one of multiple video streams for output. However, since the phrase "one to at least two" is indefinite within the context of the claim, the rejection still stands because Dunn's device can select one of the video streams for output. Therefore, this argument is moot and the rejections to claims 1-3, 13, and 17 still stand.

Regarding claims 18 and 19, the applicant did not make arguments directed to the claims. The applicant states "Claims 6, 9-12, 18, and 19 depend from claim 6", however, this is not true. Claims 18 and 19 depend from claim 17 and the rejections are therefore maintained.

2. Applicant's arguments filed 10 January 2005 regarding the rejections of claims 14-16 have been fully considered but they are not persuasive.

Regarding the arguments set forth in the second full paragraph of page 11 of the applicant's remarks, the applicant states "The alleged motivation for using FPGAs simply recites known advantages of FPGA. These advantages in no way suggest the

specifically claimed coupling of the FPGAs and claimed configuration thereof. And no evidence is provided to suggest the claimed coupling and configuration. Therefore, the alleged motivation is conclusory and improper." The Examiner made direct correlations between the specifically claimed video bus controller functionality and connections thereto in the rejection of claim 13. The statement of claim 14 was simply "wherein the video bus controller arrangement is implemented with one or more field programmable gate arrays (FPGAs)." As originally stated by the examiner, the Dunn reference is silent as to the nature of the actual elements and processors used to fulfill the processes. In other words, the Dunn reference does disclose the specific connections and functionality, however, is silent as to how the connections and functionality take place on the chip. Therefore, the examiner maintains his Official Notice that FPGAs are notoriously well known in the art to be used as typical logic chips for specialized applications. FPGAs can be programmed in any number of ways depending upon the functionality required by the implementation, not the least of which could be a simple multiplexing device. The specific connections and configurations are disclosed by Dunn, however, they are not implemented in an FPGA, the examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize FPGAs to implement the claimed video bus controller arrangement, in order to allow for easy programmability, adaptability, and flexibility while implementing the video bus. Since the Examiner maintains his Official Notice rejection, the rejections to claims 14-16 still stand.

3. Applicant's arguments filed 10 January 2005, with respect to the rejection(s) of claim(s) 20-26 under 35 USC 103(a) as being unpatentable over Dunn in view of Wicker (USP 6,441,857) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Dunn.

Regarding claim 20, the Dunn reference teaches all of that which is discussed with regards to claim 1. However, the Dunn reference does not disclose that the "second clock rate is about half of the first clock rate." The Dunn reference does disclose that the encoder operates at a 27 MHz clock rate (the first clock rate). The reference is silent as to the clock rate of the multiplexer (the second clock rate), though as mentioned in previous office actions, a clock rate of 13.5 MHz is in accordance with acceptable standards. The examiner takes Official Notice that it is notoriously well known in the art to delay the MUX clock significantly enough so that the data coming through the encoder at 27 MHz has enough time to stabilize on the encoder/digitizer output and enter the multiplexer in a reliable fashion. Therefore, a clock rate of "about half" (13.5 MHz) would easily accomplish the task. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a multiplexer clock of about half that of the encoder clock, in order to allow for data stabilization on the encoder output therefore providing proper data input to the multiplexer and a clock rate that adheres to acceptable standards.

Claims 21-26 are maintained according to the original rejection as being unpatentable over Dunn in view of Wicker (see the original rejection below).

4. Applicant's arguments filed 10 January 2005, with respect to claim 4 and 5 have been fully considered and are persuasive. Therefore, the rejection of claims 4-12 has been withdrawn.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

6. Claims 1, 20, 31, and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The term "about" in claim 20 is a relative term, which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For the purposes of this office action, the term has been ignored.

8. The term "one to at least two" in claims 1, 31, and 32 is a relative term, which renders the claims indefinite. The term "one to at least two" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For the purposes of this office action, the scope is understood to be "one to two".

Allowable Subject Matter

9. Claims 4-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 4 and its dependant's claim the "fail-safe video subsystem" of the invention. While many fail-safe systems are known to exist in the art of video delivery, by way of example, the Takamori patent (USP 5,287,186), the Chang patent (USP 6,791,601), the Reese patent (USP 5,583,796), and the Budow patent (USP 5,625,864), none of the more pertinent prior art disclose the ability to "input fail-safe analog video signals from a plurality of alternative video sources, respectively, wherein the alternative video sources are not in the first plurality of video sources". The **ability to direct alternative video streams** to the client device on a power failure or other type failure of the server is not taught in the prior art. Most prior art teachings include a "backup" or copy of the video that is sent through other means of delivery upon a power failure or other failure of the server, thereby providing the user with the same video image transmitted through different delivery means. Claims 5-12 disclose more of the details of the fail-safe system and are therefore indicated as allowable subject matter over the prior art.

10. Claims 31 and 32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. Claims 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if the rejection under 35 USC 112, 2nd paragraph of the base claim 32, as set forth in this Office action, is overcome.

12. The following is a statement of reasons for the indication of allowable subject matter: Claims 31 and 32 and its dependant claims claim the "fail-safe video subsystem" of the invention. While many fail-safe systems are known to exist in the art of video delivery, by way of example, the Takamori patent (USP 5,287,186), the Chang patent (USP 6,791,601), the Reese patent (USP 5,583,796), and the Budow patent (USP 5,625,864), none of the more pertinent prior art disclose "means for inputting a fail-safe analog video signal **from a source not in the plurality of video sources**". The **ability to direct alternative video streams** to the client device on a power failure or other type failure of the server is not taught in the prior art. Most prior art teachings include a "backup" or copy of the video that is sent through other means of delivery upon a power failure or other failure of the server, thereby providing the user with the same video image transmitted through different delivery means. Claims 33-35 disclose more of the details of the fail-safe system and are therefore indicated as allowable subject matter over the prior art.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 13, 17, 27, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Dunn et al (US Pat. No. 6,154,772), cited by examiner.

With regards to claim 1, the claimed integrated video distribution system for distributing video signals from a plurality of sources is met as follows: The claimed control bus is met by the control channel, which is present on the communication channel 16, of figure 1 and by control lines 1011 of Figure 14. As described in column 19, lines 48-56 and column 20, lines 46-49, the control channel 1011 is used to control system operation. The claimed video digitizer arrangement coupled to the control bus and having a plurality of analog video input ports and a plurality of digital video output ports, the digitizer arrangement configured and arranged to convert analog video signals to digital video data in YCrCb format at a first clock rate, each output port coupled to a respective first set of signal lines is met by MPEG-2 encoder 109, which converts received (input) analog broadcasts into (output) digitally compressed video signals. Column 7, lines 24-31 and lines 48-54 teach the use of the aforementioned MPEG-2 encoder(s). The claimed multiplexer arrangement having a plurality of output ports, each coupled to a respective second set of signal lines, the multiplexer configured and arranged to multiplex the digital video data at a second clock rate that is less than the first clock rate, wherein a number of signal lines in each first set is greater than a number of signal lines in each second set is met by the multiplexer 111 of Figure 4. As

described in column 7, lines 48-54, the multiplexer serves to multiplex the now digitally encoded video onto the video control shelf. As can be seen in Figure 4, the multiplexer has multiple "M" inputs and it only has 1 output, therefore meeting the fact that the multiplexer has more input lines than output lines. The claimed digital video bus having a plurality of video channels coupled to respective output ports of the multiplexer, wherein each channel carries a stream of video data is met by the broadcast backplane 1200 (Figure 13). The multiplexer provides MPEG-2 digital video data in parallel format to the backplane. Column 19, lines 4-23 describe the broadcast backplane and its function as a digital video bus. The claimed plurality of terminal controllers responsive to an input signal coupled to the video bus and to the control bus, each terminal controller having a data input port and a video output port and configured and arranged to select a subset of the streams of video data for output are met by the UAA modules 1000. The UAA modules function as access adapters for users to receive digital video content from the backplane and deliver the video programming to the customer as requested. Column 18, line 54 – column 19, line 23 describe, in detail, the ability for the UAA modules, acting as terminal controllers, to take input from the user and output the appropriate video content from the broadcast backplane to the user.

With regards to claim 2, Dunn teaches all of that which is discussed above with regards to claim 1. Dunn further teaches the claimed control signals being received at the UAA modules (terminal controllers) via input ports. According to column 19, lines 48-56, the UAA modules allow for user input via a control channel received at the UAA module.

With regards to claim 3, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed backplane arrangement including the video bus and the control bus and having a plurality of expansion slots for connecting to the terminal controllers, each slot having pins coupled to the video bus and to the control bus is met by column 18, lines 4-49, wherein Dunn discloses a system which has a broadcast backplane 1200, including a digital video bus and control signals. He also discloses UAA module expandability, which can provide services to new customers and can be added (inserted into expansion slots) to the broadcast backplane.

With regards to claim 13, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed digitizer arrangement comprising the following is met as follows: The claimed plurality of digitizers coupled to the analog video input ports are met by MPEG-2 encoder(s) 109, which, as described in column 7, lines 24-54, serve to digitally encode the received analog video input. The claimed plurality of digital video receivers having input ports arranged to receive input digital video signals is met by the direct reception of the digital signals by the control shelf via connection 118, as described in column 7, lines 31-34. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200.

With regards to claim 17, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed plurality of display terminals coupled to the terminal controllers are met by the customer premises' for viewing video content, which are coupled to the UAA modules (terminal controllers). Figure 16 and column 21, line 66 – column 22, line 51 describe the customer premises' and its functions in detail. The claimed plurality of input devices coupled to the terminal controllers, the input devices arranged for input of control signals to the terminal controllers to select certain ones of the video signals for display at the display terminals is met by the IR remote control interface 1358, which serves to allow control communication to the UAA and is used for the purpose of selecting videos to be displayed at customer premises'.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, in view of Chang et al (US Pat. No. 6,791,601), cited by examiner.

With regards to claim 18, Dunn teaches all of that which is discussed above with regards to claim 17. Dunn does not expressly disclose an input device being a point-and-click device, however, he does suggest user input at the subscriber premises.

Chang specifically points out the use of a pointing device for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the point-and-click device of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

With regards to claim 19, Dunn and Chang teach all of that which is discussed above with regards to claim 18. Dunn does not expressly disclose an input device being a touchscreen, however, he does suggest user input at the subscriber premises. Chang specifically points out the use of a touchscreen for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the touchscreen of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

5. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, and Chang et al (US Pat. No. 6,791,601), cited by examiner.

With regards to claim 14, Dunn teaches all of that which is discussed above with regards to claim 13. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to

process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200. The supervisory module 252, shell processor module 300, and video control module 250 are all implemented as separate entities within the system and all utilize some form of processor to accomplish their tasks. The reference, however, is silent as to the nature of the actual elements and processors used to fulfill the processes. The examiner gives Official Notice that it is notoriously well known in the art to use Field Programmable Gate Arrays (FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility, adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 15, Dunn teaches all of that which is discussed above with regards to claim 14. Dunn further discloses a system for coupling input analog signals (which have been digitized via the MPEG-2 encoder) to the video bus. He also discloses a system that couples input digital signals directly to the video bus. Column 7, lines 24-34 provide a brief explanation of this teaching. Dunn is silent as to the exact means of coupling involved. He does disclose that certain parts are present (such as the video control shelf and connections 118), however, he does not expressly disclose how these couplings and connections are made. The examiner gives Official Notice that it is notoriously well known in the art to use Field Programmable Gate Arrays

(FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility, adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 16, Dunn and Chang teach all of that which is discussed above with regards to claim 14. Dunn further teaches a system that can multiplex and combine programming so as to increase and fully utilize available bandwidth in the network (column 9, lines 5-15). The claimed video channels being comprised of a first and a second set of video channels, each channel of the first set having a number of signals sufficient for parallel transmission of multiple streams of monochrome video data is met by the transmission of multiple program groups (as discussed in column 9, lines 5-15), which can be monochrome vs. color, or any other form of grouping that is preferred for transmission. The claimed second set having a number of signal lines sufficient for transmission of a single stream of color video data is met by the same connection with the same program groups, which get multiplexed on the transmission line.

6. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, in view of Wicker et al (US Pat. No. 6,441,857), cited by examiner.

With regards to claim 21, Dunn and Wicker teach all of that which is discussed above with regards to claim 20. Dunn does not disclose the a video data multiplexer

arrangement generates data that defines a color pixel, each pixel defined by at least four words of data and a color video control code. This claim, however, is met by Wicker, wherein he teaches a 16-bit 4:2:2 YCrCb pixel data processing apparatus (column 10, lines 7-22). As can be seen, each pixel is defined by 4 4-byte words and a color video control code (see Figure 6). It would have been obvious to one or ordinary skill in the art at the time of the invention to implement to 16-bit 4:2:2 YCrCb pixel data processor into the multiplexer taught by Dunn, in order to allow for a standardized transmission scheme. YCrCb data is commonly known in the art and is a standard way of transmitting Luminance and Chrominance values, which define an image.

With regards to claim 22, Dunn and Wicker teach all of that which is discussed above with regards to claim 21. Dunn does not expressly disclose that the data words are transmitted on different clock edges. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the 16-bit YCrCb Mode is transmitted. The first and third data words (CrCb 0-7) are transmitted on the rising edge and the second and fourth data words (Y0-Y7) are transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

With regards to claim 23, Dunn and Wicker teach all of that which is discussed above with regards to claim 22. Dunn does not expressly disclose anything about the data words. Wicker discloses a system that uses the first and second words to define chroma red data, the third and fourth data words to define the chroma blue data, and all four data words to define the luma data. Column 10, lines 7-22 and Figure 6, show that the data is broken up into words and transmitted accordingly. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the Dunn system in order to transmit the chroma red, chroma blue, and luma data to define a pixel. This would have provided the benefit of a standard transmission scheme and the ability for the information to be easily transmitted without the need for a large amount of bandwidth.

With regards to claim 24, Dunn and Wicker teach all of that which is discussed above with regards to claim 23. Dunn does not disclose a specific frequency at which the data words are clocked at the multiplexer. Wicker, however, discloses a frequency of 27 MHz, which is double that utilized by the encoders. This meets the claimed data words being clocked at a frequency of 33 MHz, since 33 MHz and 27 MHz do not provide a patentable distinction. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specified frequency to clock data words into the multiplexer within the system as taught by Dunn in order to utilize a frequency that is double that of the encoder frequency and to allow the system to work at a higher clock rate.

With regards to claim 25, Dunn and Wicker teach all of that which is discussed above with regards to claim 20. Dunn does not disclose anything about the multiplexer arrangement generating data that defines monochrome pixels, each pixel being defined by a set of data words and a monochrome video control code. This claim, however, is met by Wicker, wherein he teaches a 16-bit 4:2:2 YCrCb pixel data processing apparatus (column 10, lines 7-22), which can also be used to process monochrome pixel data. As can be seen, each pixel is defined by 4, 4-byte words and a video control code (see Figure 6). It would have been obvious to one or ordinary skill in the art at the time of the invention to implement to 16-bit 4:2:2 YCrCb pixel data processor into the multiplexer taught by Dunn, in order to allow for a standardized transmission scheme. YCrCb data is commonly known in the art and is a standard way of transmitting Luminance and Chrominance values, which define an image.

With regards to claim 26, Dunn and Wicker teach all of that which is discussed above with regards to claim 25. Dunn does not expressly disclose the data words being transmitted on a rising clock edge and a falling clock edge. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the 16-bit YCrCb Mode is transmitted. The first data word (CrCb 0-7) is transmitted on the rising edge and the second data word (Y0-Y7) is transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance

values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reese (USP 5,583,796) discloses a system to provide backup video to a client for switching the same video through different delivery means upon a failure at the main switch.

Budow et al (USP 5,625,864) disclose a system for providing VOD or PPV in a hotel-like environment. Column 4, lines 40-45 disclose a backup video system in case the server fails.

Takamori (USP 5,287,186) discloses a system for switching backup video through to the client in case of a failure of the main switch.

Chang et al (USP 6,791,601) disclose a system for re-routing video output to a display upon power failure in the main switching unit of an endoscope system. The Chang reference only utilizes one input, however.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R. Shannon who can be reached at (571) 272-7356 or Michael.Shannon@uspto.gov. The examiner can normally be reached by phone Monday through Friday 8:00 AM – 5:00PM, with alternate Friday's off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (571) 272-7353.

Any response to this action should be mailed to:

Please address mail to be delivered by the United States Postal Service (USPS) as follows:

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Or faxed to: (703) 872-9306

Hand-delivered responses should be brought to:

Knox Building
501 Dulany Street

Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is **(571) 272-2600**.

Michael R Shannon
Examiner
Art Unit 2614

Michael R Shannon
June 10, 2005

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600